A COMPACT AND LOW POWER DIGITAL TO ANALOG CONVERTER FOR HEARING AID APPLICATIONS

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Introduction:

Hearing loss can significantly impede communication, which is essential for human interaction. It has a profound negative impact on various aspects of life, including work, physical and emotional well-being, and relationships. In fact, it is considered the third most common health issue affecting relationships and overall quality of life. Hearing aid devices play a crucial role in addressing hearing impairment by selectively amplifying sound signals to accommodate the unique hearing characteristics of each individual. Despite their benefits, there exists a considerable disparity between the potential and actual users of hearing aids. While digital hearing aids with reconfigurable filter banks have been developed, they often come with a hefty price tag, making them inaccessible to many. In order to provide a more accessible solution, our project aims to design a low-cost low-power hearing aid device that is more affordable.

Objectives:

1. Characterization of various memristor models to get the required characteristics for Data converter design.
2. Design and implementation of 2-bit DAC and 4-bit DAC using memristor (MatLab and Cadence) and compare the performance metrics- INL, DNL, SFDR, Power, ENOB, etc. reported in the literature.
3. Design and implementation of 8-bit DAC using a Memristor array and compare with the performance metrics of the existing 8-bit DAC architecture used in hearing aid applications.
4. Characterization of memristor-based 8-bit DAC architecture to improvise the performance metrics suitable for hearing aid devices
5. Development of low cost and low power hearing aid device using memristor

Methodology:

Figure 1 depicts the basic block diagram of a hearing aid device. This project focuses on the DAC and the buffer architecture. The proposed design aims to introduce a low-cost, low-power, and compact hearing aid device that is more affordable. As part of this effort, the design includes a digital-to-analog converter utilizing memristors to reduce power consumption within the hearing aid device. This project involves

- Detailed literature survey on the existing low-cost hearing aid devices and their design.
- Detailed literature survey on various memristor models and their characteristics.
- Testing the characteristics of memristor models using Cadence Virtuoso and MatLab to compare with the results in the literature and fixing the device constants based on the characteristics.
- Implementation of memristor-based 2-bit and 4-bit Digital analog converter (DAC) reported in the literature and compared with the results to validate the methodology
- Design, Implementation and characterization of a novel DAC architecture which is very compact and low power with 8-bit resolution using memristors that matches with the specification required for hearing aid devices.

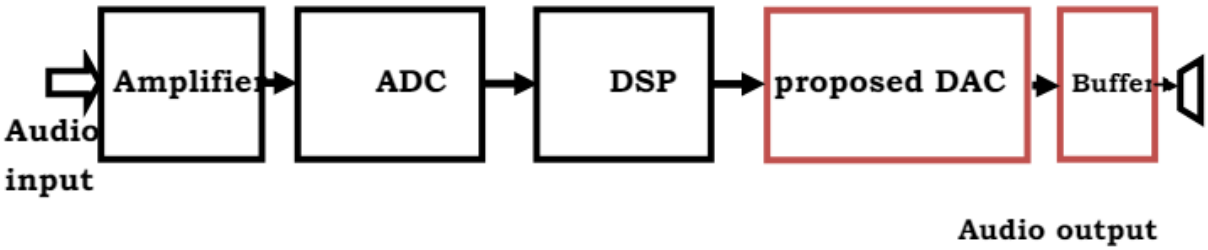

Figure 1

- Testing the proposed DAC architecture with real-time input signal data.
- Design and implementation of CMOS Buffer amplifier to drive the output peripheral device.
- Testing of the design with hardware circuit.

Conclusion:

Basic hearing aid device with adjustable volume control is designed and implemented using the discrete components to understand the properties of audio signal, the signal swing required at the output to make it audible for the user, power requirement and the challenges.
Figure 2 represents the hardware model of the basic hearing aid system with two amplifier stages flowed by feedback amplifier stage and a power amplifier to drive the headphone of 32 Ohm impedance.

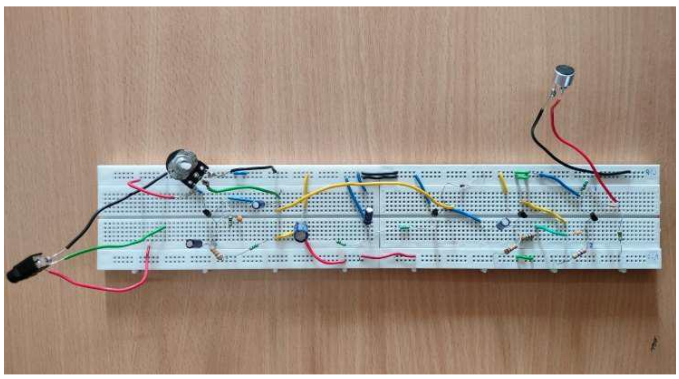

Figure 2

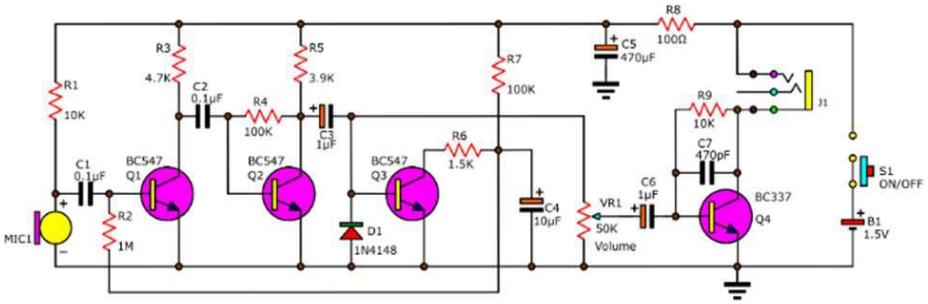

Figure 3

Stage 1:

Basic hearing aid circuit with discrete components to drive 32 Ohm load is implemented and tested in real-time. The circuit is designed for 1.0 V DC power supply, which is able to provide 0.25 Vpp as maximum output swing across 32 Ohm. Figure 4 represents the output signal obtained across 32 Ohm load. The output obtained from the feedback stage is saved in excel sheet using NI ELVIS III kit and this data is used to verify the designed DAC circuit in Cadence.

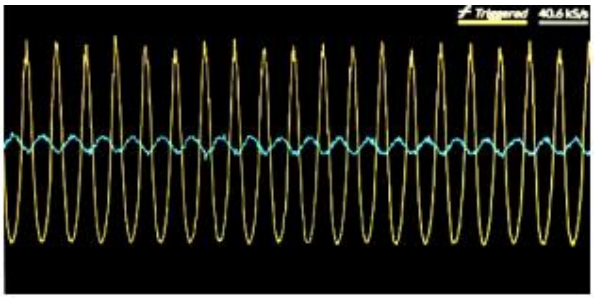

Figure 4

Stage 2

8-bit memristor-based binary weighted DAC is designed and implemented in Cadence Virtuoso tool and is found to have an SNR of 47.93 dB and a resolution of 8 bits at 10 kHz. The proposed DAC is designed using the VTEAM memristor model. Simulations verified that the required on and off resistance to implementing the memristive DAC is 200 Ω and 16 kΩ respectively. The simulation results depict that the proposed DAC consumes a power of 9.89 µW for a digital input voltage 1 V and

CL= 1 pF and $R¬L = 100 kΩ and uses 75 memristors that approximately occupy an area of 4800 nm2. An overall area reduction of 40 % is achieved by the 8-bit memristor DAC when compared to the conventional binary-weighted DAC architecture using resistor. As majority of the hearing aid devices have an output impedance less than 100 Ω. In order to drive a load resistance of less than 100 Ω, there is a need for a class D buffer amplifier with supply 1 V in order to get the desired output with minimum distortion and noise. This Class D buffer amplifier will be integrated along with the memristor based to obtain a complete hearing aid device.

Innovation in the project

Memristor based circuit design can reduce the power consumption as well as area. Various DAC architectures use resistor strings to convert the digital signal to an analog signal. Here, we propose the DAC architecture using memristor array that can reduce the overall DAC area by 40 % and the power consumption can be reduced drastically. Portable devices like hearing aids require low power and compact designs. This project proposes the memristor based DAC architecture for hearing aid devices.

Future Scope

Memristor based flash ADC design and reconfigurable filter design can be incorporated in the hearing aid architecture, thereby reduces the overall power as well as area.